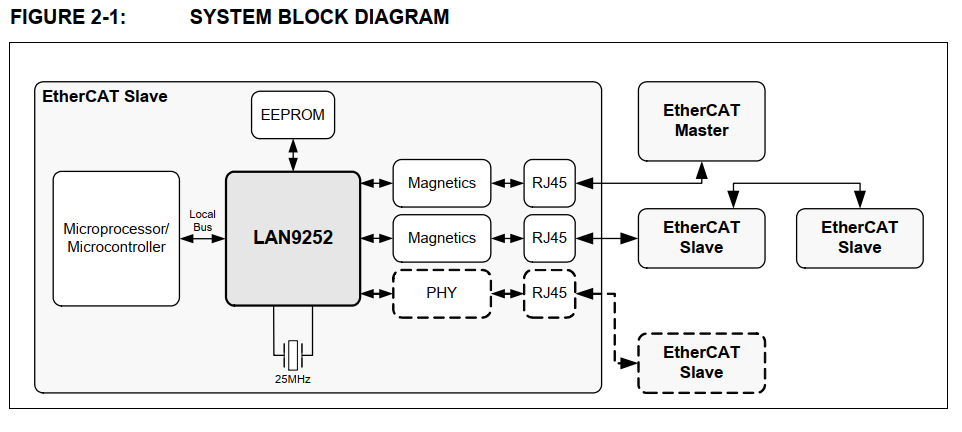
Ethercat Implementation

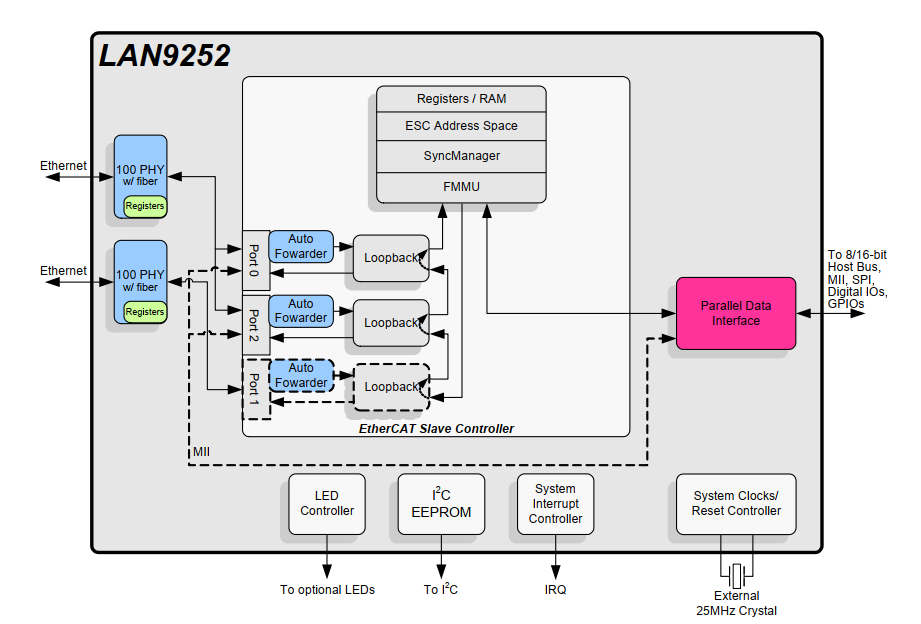
Device featured: Microchip DEVB-LAN9252-SPI

The SPI bit lanes are supported with a clock rate up to 80MHz

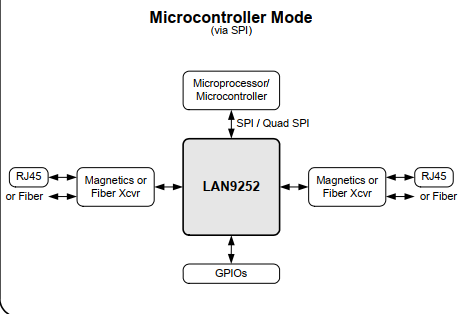
The following is the system block diagram from (Microchip), taking into account that the Microcontroller will be the Nucleo-F446ZE and the EtherCAT Master will be a PLC/IPC from Beckhoff.



The Internal diagram of the chip:



The following is the operation mode in which an external microcontroller uses a SPI or Quad-SPI to communicate and control the EtherCAT Slave.



Regarding the implementation of the Protocol Stack

It might be possible that a licensed stack is needed such that the device can be certified as official compatible EtherCAT device.

<https://www.ethercat.org/en/products/54FA3235E29643BC805BDD807DF199DE.htm>